REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-9 are presently pending in this application, Claims 1 and 7 having been amended by the present amendment.

In the outstanding Office Action, Claims 1-3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gorczyca, et al. (U.S. Patent 5,161,093) in view of Wojnarowski, et al. (U.S. Patent 5,366,906); and Claims 4-5 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gorczyca, et al. in view of Wojnarowski, et al., and further in view of Sunahara (U.S. Patent 6,153,290).

However, Claims 6-9 were allowed. Applicant acknowledges with appreciation the indication of allowable subject matter.

Amended Claim 1 is fully supported by the specification, drawings and claims as originally filed.[1] Claim 7 has been amended to correct a typographical error. Thus, no new matter has been introduced.

Briefly recapitulating, Claim 1 is directed to a printed circuit board arrangement. For example, referring to the non-limiting embodiment of Fig. 8, the printed circuit board arrangement includes a core substrate 30 having a cavity, a resin insulating layer and a conductor circuit laminated on the core substrate, an IC chip having an electrode, and a plurality of capacitors 20 accommodated in the cavity. The IC chip is mounted on an outer layer of the conductor circuit, and the electrode of the IC chip faces and is connected to the solder bump provided on the conductor circuit and located right under the IC chip. The capacitors are located immediately below the IC chip. Therefore, according to the present

[1] For example, Figs. 8 and 15 of the present application.

invention recited in Claim 1, the conductor line distance between the capacitor and the IC chip can be reduced.

The Office Action asserts that Gorczyca et al., referring to Fig. 3, disclose a core substrate having a cavity, a resin insulating layer, a conductor circuit laminated on the core substrate, and a plurality of capacitors accommodated in the cavity. However, the Office Action admits that Gorczyca, et al. do not disclose an IC chip mounted on an outer layer of the conductor circuit, the IC chip being connected via a solder bump located under the IC chip, and the capacitors being located immediately below the IC chip.

Indeed, Gorczyca et al. fail to disclose that an IC chip is mounted on an outer layer of the conductor circuit, that the electrode of the IC chip faces and is connected to the solder bump that is provided on the conductor circuit and located right under the IC chip, and that the capacitors are located immediately below the IC chip.

The Office Action further asserts that Wojnarowski et al. disclose a wafer including an IC chip mounted on an outer layer of a conductor circuit, the IC chip being connected via a solder bump, and chips including an IC's and single components being located immediately below the IC chip.

However, Wojnarowski et al. fail to disclose that the electrode of the IC chip faces and is connected to the solder bump that is provided on the conductor circuit and located right under the IC chip. Instead, Wojnarowski et al. disclose that, referring to Fig. 7, the IC chip 74 is mounted on the wafer 10 by **TAB** 72 or **wire bonding**[2], which is different from the limitation that "the electrode of the IC chip facing and being connected to the solder bump located right under the IC chip" recited in Claim 1. Therefore, in the Wojnarowski et al. printed circuit board, the conductor line distance between the capacitors and the IC chip cannot

[2] Wojnarowski et al., col. 10, lines 25-31.

be reduced.

Since neither Gorczyca et al. nor Wojnarowski et al. teach that the electrode of the IC chip faces and is connected to the solder bump that is provided on the conductor circuit and located right under the IC chip, even if the teachings of these references are combined, the combined teachings of these references would not in any way obviate the invention recited in Claim 1.

None of the applied references, including Wojnarowski et al., provides the motivation to modify the Gorczyca et al. printed circuit board so as to arrive at Applicants' claimed invention.[3] In rejecting a claim under 35 U.S.C. 103(a), the USPTO must support its rejection by "substantial evidence" within the record.[4] There is no substantial evidence within the record of motivation for modifying the admitted prior art device so as to obtain Applicants' claimed invention. Therefore, Claim 1 is believed to be allowable.

Substantially the same arguments as set forth above with regard to Claim 1 also apply to dependent Claims 2-5, which depend directly or indirectly from Claim 1. Accordingly, each of the dependent claims is also believed to be allowable.

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[3] See MPEP 2143.01 stating "[o]bviousness can only be established by combining or modifying the teaching of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art," (citations omitted). See also MPEP 2144.08 III stating that "[e]xplicit findings on motivation or suggestion to select the claimed invention should also be articulated in order to support a 35 U.S.C. 103 ground of rejection. . . Conclusory statements of similarity or motivation, without any articulated rational or evidentiary support, do not constitute sufficient factual findings."

[4] In re Gartside, 203 F3d 1305, 53 USPQ2d 1769 (Fed. Cir. 2000) (holding that, consistent with the Administrative Procedure Act at 5 USC 706(e), the CAFC reviews the Board's decisions based on factfindings, such as 35 U.S.C. 103(a) rejections, using the substantial evidence' standard because these decisions are confined to the factual record compiled by the Board.)

Consequently, in view of the present amendment, it is respectfully submitted that this application is in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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